REMARKS

Claims 1-76 remain in the application. No claims have been amended. No claims have been canceled. No claims have been added.

Information Disclosure Statement

Applicant is submitting herewith a PTO 1449 form and associated references. Applicant wishes to draw the Examiner's attention to the following reference on that form:

> "The Distributed Clock Generator" by Scott Fairbanks, Simon Moore, Computer Laboratory, University of Cambridge, UK (December 5, 2001)

Applicant respectfully submits that the description of the claimed invention contained therein is attributable to the inventor of this application and does not qualify as prior art.

Examiner Interview

Applicant wishes to thank the Examiner for his time for the Examiner telephone interview on May 19, 2005; during which the Applicant and the Examiner reached agreement that the rejections in the Office Action have been overcome by the arguments presented below.

Drawings

The drawings corresponding to claim 6 are objected to on the basis that the following features: "each of different parts of synchronous logic is coupled through one or more amplifiers to a different one of the clock wires of the clock generator" are missing. Applicant respectfully submits that examples of the amplifiers (which are optional – see paragraph 0052) as referenced in claim 6 are shown in at least Figures 3

and 5. The optional amplifiers are purposely omitted from certain other Figures to reduce clutter (e.g., see paragraph 0057 and Figure 4; paragraph 0062 and Figure 7).

The drawings corresponding to claim 11 are objected to on the basis that the following features: "a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein the plurality of set of synchronous logic are interconnected" are missing. With regard to the interconnected synchronous logic of claim 11, Applicant respectfully submits that examples of the possibility of interconnected synchronous logic are shown in at least Figures 3, 4, 5 and 7 as described in the specification in at least paragraphs 0044 and 0052. Specifically, Applicant respectfully submits that the possibility of interconnected synchronous logic driven by a distributed clock is generally understood by those skilled in the art and is a "conventional feature", within the meaning as defined in 37 CFR 1.83(a); and is thus represented graphically for example, by the space outside the cells in at least Figures 3, 4, 5 and 7.

Claims 1-4 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bushman et al. (U.S. Patent No. 6,657,502).

Independent claim 1:

Independent claim 1 includes the element of "a clock generator, distributed over an integrated circuit, including a plurality of cells each coupled to multiple adjacent ones of said plurality of cells by different clock wires, wherein, for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge." (Emphasis added).

Bushman discloses a multiphase quadrature Voltage Controlled Oscillator (VCO), which can be integrated onto a single integrated circuit chip producing at least two output clock signals 90 degrees out of phase with each other.

Bushman describes in Figure 6 a VCO configuration consisting of four cells (e.g., cell 1 = 134' and 134"; cell 2 = 136' and 136"; cell 3 = 138' and 138" etc.), each consisting of a pair of inverter amplifiers, where each inverter amplifier may be implemented as illustrated in Figure 7A, 7B, or 7C. By way of example, the outputs of 134' and 134" are coupled together to form the output of cell 1 and provide the inputs to 136" and 138'. The cell consisting of 134' and 134" generates both the rising and falling edge of the clock on line Q (at node 142), which is the input to both: 1) the cell consisting of 138' and 138"; and 2) the cell 136' and 136". By using Figure 7A as a specific example, the output 156 of both 134' and 134" (collectively forming cell 1) generates the rising and falling edge with V_{dd} and V_{ss}; while the input of both 138' and 136" simply receive that clock. Thus, in contrast to Applicant's claim 1 where "for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge", Bushman's VCO in Figure 6 illustrates that a cell on one end of a clock wire generates both the rising and falling edges, but the two cells on the other end of the same wire only receive and cannot generate a rising or falling edge with respect to that clock wire. This is equally true for each cell represented by a pair of inverter amplifiers in any configuration represented in Figures 7A – 7C. In other words, none of the inverter amplifiers can generate either a rising or falling edge on the wire labeled as input in Figures 7A, 7B, and 7C. Therefore, in Bushman's VCO, for each of a plurality of clock wires, only <u>one cell</u> on one end generates <u>both</u> the rising and falling edge.

Furthermore, Bushman does not make obvious claim 1 either. The distinction discussed above is made more apparent in view of Bushman's goal of generating multiple clocks (with different phases). In contrast, an advantage of the limitations of claim 1 is a clock generator distributed over the integrated circuit with cells that may work together to synchronize the phase of a clock signal.